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OUTPUT BUFFER CIRCUITS INCLUDING LOGIC GATES HAVING BALANCED OUTPUT NODES

Abstract of the Disclosure

A buffer circuit may include an output terminal, a pull-up transistor, a pull-down transistor, and first and second logic gates. The pull-up transistor is connected between the output terminal and a supply voltage, and the pull-up transistor pulls the output terminal up to the supply voltage responsive to a pull-up control signal. The pull-down transistor is connected between the output terminal and a reference voltage, and the pull-down transistor pulls the output terminal down to the reference voltage responsive to a pull-down control signal. The first logic gate may generate the pull-up control signal at a first output node responsive to a control signal and a data signal, and the first logic gate may include a plurality of serially connected transistors in an electrical path between the supply voltage and the first output node. The second logic gate may generate the pull-down control signal at a second output node responsive to the data signal and an inverse of the control signal, and the second logic gate may include a plurality of serially connected transistors in a path between the supply voltage and the second output node.